Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 – 54 (canceled)

55. (currently amended) A chip package comprising:

~~a semiconductor device;~~

a substrate having a first side and a second side opposite to said first side, wherein said substrate comprises multiple contact points at said second side, ~~comprising~~ a solder mask at said first side, an interconnect covered by said solder mask and a first metal pad exposed by an opening in said solder mask; ~~separate from said solder mask, wherein said first pad is at a horizontal level same as said solder mask is at, and wherein said first pad has a circular shape;~~

a chip over said first side of said substrate, wherein said chip comprises a silicon substrate, multiple layers of interconnecting lines comprising copper, multiple insulating layers comprising an oxide material, multiple metal vias in said multiple insulating layers and between said multiple layers of interconnecting lines, wherein said multiple metal vias are connected to said multiple layers of interconnecting lines, and a polymer layer, wherein an opening in said polymer layer exposes a second metal pad of said multiple layers of interconnecting lines;

a ~~metal~~ copper pillar between ~~said semiconductor device and~~ said first and second pads, ~~pad,~~ wherein said copper pillar is connected to said second metal pad through said opening in said polymer layer, and wherein said ~~metal~~ copper pillar has a thickness between 10 and 100 micrometers;

a titanium-containing layer between said second metal pad and said copper pillar, wherein said titanium-containing layer is on said second metal pad, on said polymer layer and in said opening in said polymer layer;

~~an under bump metal layer between said metal pillar and said first pad, wherein said metal pillar has a transverse dimension smaller than that of said under bump metal layer, wherein said metal pillar has a first sidewall recessed from a second sidewall of said under bump metal layer, wherein a distance between said first sidewall and said second sidewall is greater than 0.2 micrometers, and wherein said under bump metal layer comprises a first portion over said metal pillar and a second portion overhanging said metal pillar;~~

a solder metal between said ~~under bump metal layer~~ copper pillar and said first metal pad, wherein said solder metal is connected ~~bonded~~ to said first metal pad; ~~and~~

a nickel-containing layer between said copper pillar and said solder metal; and

an underfill between said chip ~~semiconductor device~~ and said first side of said substrate, wherein said underfill contacts with said chip ~~semiconductor device~~ and said first side of said substrate and encloses said ~~metal~~ copper pillar ~~and said solder metal~~.

Claim 56 (canceled)

57. (currently amended) The chip package of Claim 55, wherein said substrate further comprises multiple third metal ~~second~~ pads exposed by said opening in said solder mask, ~~at said horizontal level, wherein each of said multiple second pads has said circle shape,~~ wherein said solder mask is separate from said first metal pad and from said multiple third metal ~~second~~ pads, and wherein said first metal pad and said multiple third metal ~~second~~ pads are aligned in a direction parallel with a sidewall of said opening in said solder mask.

58. (currently amended) The chip package of Claim 55, wherein said copper pillar has a transverse dimension smaller than that of said nickel-containing layer, wherein said copper pillar has a first sidewall recessed from a second sidewall of said nickel-containing layer, wherein a distance between said first sidewall and said second sidewall is greater than 0.2 micrometers, and wherein said nickel-containing layer comprises a first portion over said copper pillar and a second portion overhanging said copper pillar. ~~said semiconductor device comprises a second pad and a passivation layer, wherein said second pad is exposed by an opening in said passivation layer, and wherein said metal pillar is between said second pad and said first pad.~~

Claim 59 (canceled)

60. (previously presented) The chip package of Claim 55, wherein said substrate comprises a ball grid array substrate.

61. (currently amended) The chip package of Claim 55, where said multiple contact points comprise multiple contact balls at said second side. ~~further comprising a contact ball under said substrate, wherein said semiconductor device is over said substrate.~~

62. (currently amended) The chip package of Claim 55, wherein said first metal pad has a circular shape. ~~substrate comprises multiple second pads at said horizontal level, wherein each of said multiple second pads has said circular shape, wherein said solder mask is separate from said multiple second pads, and wherein said first pad and said multiple second pads are aligned in a direction parallel with an edge of said substrate.~~

Claims 63-65 (canceled)

66. (new) The chip package of Claim 55, wherein said nickel-containing layer has a thickness between 1 and 10 micrometers.

67. (new) The chip package of Claim 55, wherein said titanium-containing layer comprises titanium nitride.

68. (new) The chip package of Claim 55, wherein said copper pillar is electroplated.

69. (new) A chip package comprising:

a substrate having a first side and a second side opposite to said first side, wherein said substrate comprises multiple contact points at said second side, a solder mask at said first side, an interconnect covered by said solder mask and a first metal pad exposed by an opening in said solder mask;

a chip over said first side of said substrate, wherein said chip comprises a silicon substrate, multiple layers of interconnecting lines comprising copper, multiple insulating layers comprising an oxide material, multiple metal vias in said multiple insulating layers and between said multiple layers of interconnecting lines, wherein said multiple metal vias are connected to said multiple layers of interconnecting lines, and a polymer layer, wherein an opening in said polymer layer exposes a second metal pad of said multiple layers of interconnecting lines;

a copper pillar between said first and second pads, wherein said copper pillar is connected to said second metal pad through said opening in said polymer layer, and wherein said copper pillar has a thickness between 10 and 100 micrometers;

a barrier layer between said second metal pad and said copper pillar, wherein said barrier layer is on said second metal pad, on said polymer layer and in said opening in said polymer layer;

a solder metal between said copper pillar and said first metal pad, wherein said solder metal is connected to said first metal pad;

a nickel-containing layer between said copper pillar and said solder metal; and

an underfill between said chip and said first side of said substrate, wherein said underfill contacts with said chip and said first side of said substrate and encloses said copper pillar.

70. (new) The chip package of Claim 69, wherein said substrate further comprises multiple third metal pads exposed by said opening in said solder mask, wherein said solder mask is separate from said first metal pad and from said multiple third metal pads, and wherein said first metal pad and said multiple third metal pads are aligned in a direction parallel with a sidewall of said opening in said solder mask.

71. (new) The chip package of Claim 69, wherein said copper pillar has a transverse dimension smaller than that of said nickel-containing layer, wherein said copper pillar has a first sidewall recessed from a second sidewall of said nickel-containing layer, wherein a distance between said first sidewall and said second sidewall is greater than 0.2 micrometers, and wherein said nickel-containing layer comprises a first portion over said copper pillar and a second portion overhanging said copper pillar.

72. (new) The chip package of Claim 69, wherein said substrate comprises a ball grid array substrate.

73. (new) The chip package of Claim 69, where said multiple contact points comprise multiple contact balls at said second side.

74. (new) The chip package of Claim 69, wherein said first metal pad has a circular shape.

75. (new) The chip package of Claim 69, wherein said nickel-containing layer has a thickness between 1 and 10 micrometers.

76. (new) The chip package of Claim 69, wherein said copper pillar is electroplated.